Applications of New Precision Op Amps

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Two new precision bipolar op amps, the LT1001 and a dual version, the LT1002, expand applications possibilities for designers of measurement and control circuits. These devices will find use where high accuracy and/or microvolt level capability are required. A summary of the new op-amp specifications appears in Table A. The high performance of these devices makes them useful as building blocks in precision circuitry. Figure 1 furnishes an excellent example.

Table A. LT1001A Specifications

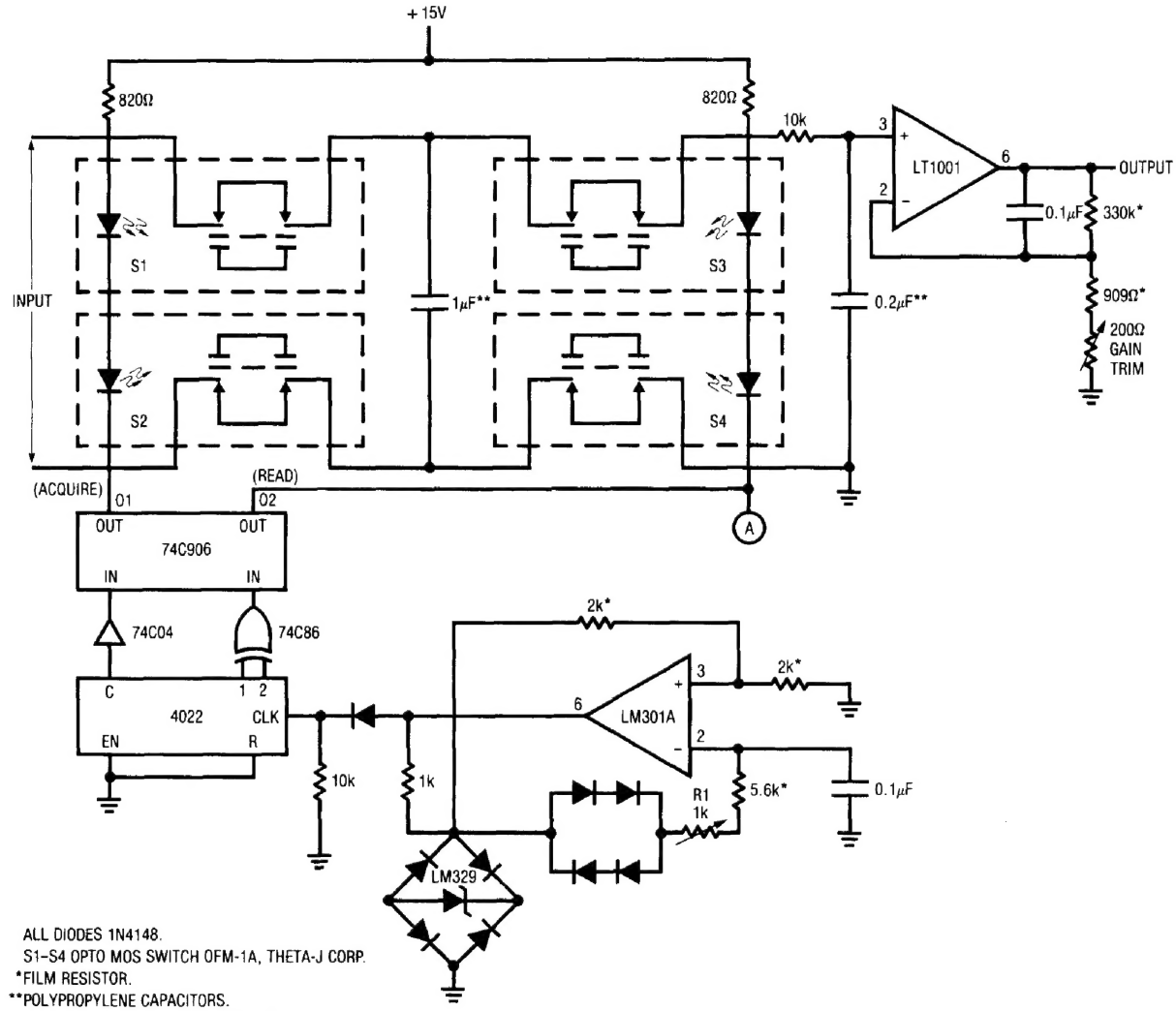
OFFSET VOLTAGE	
Initial	25μV Max
vs Temperature	1μV/°C Max
vs Time	1μV/Month Max
BIAS CURRENT	
Initial	2nA Max
Offset	2nA Max
OPEN LOOP GAIN	400,000 Min
COMMON-MODE REJECTION (+13V)	114dB Min
POWER SUPPLY REJECTION	110dB Min
SLEW RATE	0.15V/μs Min
GAIN-BANDWIDTH PRODUCT	0.5MHz Min
NOISE (Voltage)	
0.1Hz–10Hz	0.5μVp-p
10Hz	$18nV/\sqrt{Hz}$ Max
100Hz	$13nV/\sqrt{Hz}$ Max
1000Hz	$11nV/\sqrt{Hz}$ Max
NOISE (Current)	
0.1Hz–10Hz	30pAp-p Max
10Hz	0.8pAp-p Max
100Hz	0.23pAp-p Max
1000Hz	0.17pAp-p Max

Instrumentation Amplifier with $V_{CM} = 300V$ and CMRR > 160dB

The circuit of Figure 1 may be used wherever differential inputs are required. It is particularly applicable to transducer signal conditioning where high common-mode voltages may exist. The circuit has the low offset and drift of the LT1002, but also incorporates a novel switched-capacitor "front end" to achieve some specifications not available in an instrumentation amplifier. Common-mode rejection ratio at DC for the front end exceeds 160dB. The amplifier will operate over a ±300V common-mode range and gain accuracy and stability are limited only by external resistors. The high common-mode voltage capability of the design allows it to withstand transient and fault conditions often encountered in industrial environments.

The circuit's inputs are fed to LED-driven optically-coupled MOSFET switches, S1 and S2. Two similar switches, S3 and S4, are in series with S1 and S2. A2, a precision oscillator, and its associated CMOS logic functions generate non-overlapping clock outputs which drive the switch's LEDs. When the "acquire pulse" is low, S1 and S2 are on and the 1μF capacitor acquires the differential voltage at the bridge's output. During this interval, S3 and S4 are off. When the acquire pulse rises, S1 and S2 begin to go off. After a delay to allow S1 and S2 to fully open, the "read pulse" goes low, turning on S3 and S4. Now, the 1μF capacitor appears as a ground-referred voltage source which is read by the main amplifier, A3. The 10k-0.2μF network allows A3's input to retain the 1μF unit's value when the circuit returns to the acquire mode. A3 provides the circuit's output. Its gain is set in normal fashion by feedback resistors. The 0.1μF feedback capacitor sets a rolloff of 5Hz. Several features aid circuit operation. A2 is trimmed for a 93Hz clock output. This frequency inhibits power line-originated noise from interacting with the switching action because it is not harmonically related to 60Hz. Such interaction may cause DC errors.

The differential-to-single-ended transition performed by the switches and capacitors means that A3 never sees the input's common-mode signal. The 300V breakdown specification of the optically-driven MOSFET switch allows the circuit to withstand and operate at common-mode levels of ±300V (switch leakage typically rises above 1nA over 100V, causing some circuit performance degradation). In addition, the optical drive to the



ALL DIODES 1N4148.
S1–S4 OPTO MOS SWITCH OFM-1A, THETA-J CORP.
*FILM RESISTOR.
**POLYPROPYLENE CAPACITORS.
ADJUST R1 FOR 93Hz AT TEST POINT A.
A FLYING CAPACITOR CHARGED BY CLOCKED PHOTO-DRIVEN FET SWITCHES CONVERTS A DIFFERENTIAL SIGNAL AT A HIGH COMMON-MODE VOLTAGE TO A SINGLE-ENDED SIGNAL AT THE LT1001 OUTPUT.

Figure 1. Instrumentation Amplifier with 300V Common-Mode Range

MOSFETs eliminates the charge injection problems common to FET switched capacitive networks. The 750μs switching speed of the optical switch limits the circuit carrier to low frequencies, but most transducer circuits do not require any substantial bandwidth.

Linearized Platinum RTD Signal Conditioner

Platinum resistance temperature detectors (RTD) are generally accepted as the best choice for high accuracy and stability in temperature measurements. Unfortunately, they exhibit a non-linear temperature versus resistance characteristic which complicates signal conditioning. Over a 0°C to 100°C range this non-linearity amounts to 0.4°C. Figure 2 shows a thermometer circuit which corrects for this error and achieves ±0.025°C absolute accuracy over the 0°C–100°C range.

A1 functions as a negative gain inverter to drive a constant current through the platinum sensor. The LT1009 and the 10k resistor provide the current reference. Because A1 operates at negative gain, the voltage across the RTD is low and self-heating induced errors are reduced. A1's output potential, which varies with the

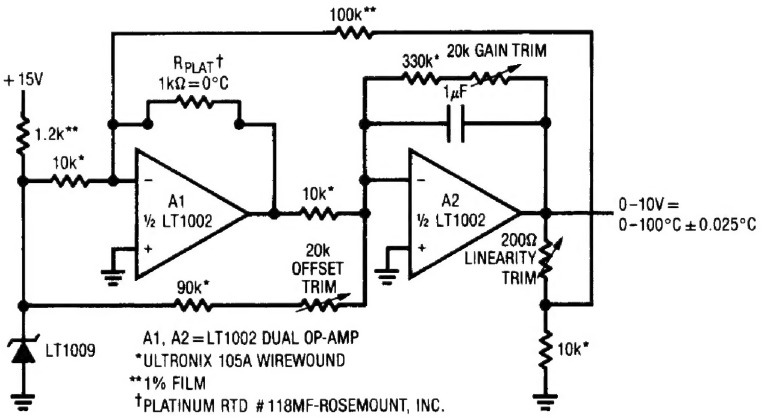


Figure 2. Linear Thermometer

platinum sensor's temperature, feeds A2. A2 provides scaled gain and offsetting so that its output will swing from 0.00V to 10.000V for a 0.00°C to 100.00°C temperature swing at the RTD. The 1μF capacitor limits noise pick-up. Normally, this circuit would exhibit a 0.4°C non-linearity error due to the RTD's imperfect response. This term is corrected by returning a small portion of the circuit's output to A1's negative input. This varies the reference current, causing compensatory changes in the circuit's gain slope. To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432-K) for the sensor. Set the box to the 0°C value (1000.0Ω) and adjust the offset trim for a 0.000V output. Next, set the decade box for a 35°C output (1138.7Ω) and adjust the gain trim for a 3.500V output reading. Finally, set the box to 1392.6Ω (100.00°C) and trim the linearity adjustment. Repeat this sequence until all three points are fixed. Total error over the entire range will be within ±0.025°C. The resistance values given are for a nominal 1000.0Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 1000.0Ω. This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Thermally Controlled Ni Cad Charger

Charging Ni Cad batteries at high current rates is desirable because it allows short charge time. The difficulty with such operations is that excessive internal heating degrades the batteries and can cause gas venting to the outside atmosphere. Schemes based on monitoring cell voltage during charge suffer because cell voltage is not necessarily indicative of the charge state of the battery. Open loop techniques involving high charge rates for a fixed time do not account for battery characteristic shifts over life and ambient temperature.

One way to charge batteries rapidly without abuse is to measure cell temperature and taper the charge accordingly. Figure 3 uses a thermocouple for this function. A second thermocouple nulls out the effects of ambient temperature. The LT1001 amplifier furnishes the low level capability necessary to work with the microvolt level thermocouple signals. To understand the circuit's operation, assume a discharged battery pack in the Darlington collector line. The battery and ambient thermocouples are at the same temperature. The battery thermocouple is directly mounted to one of the cells in the pack. The ambient thermocouple is exposed to ambient temperature and mounted to a thermal mass which approximates that

of the battery pack. Under these conditions, the thermocouple voltages cancel and the positive input is at zero volts. The negative current through the 620kΩ resistor to the summing junction causes the amplifier to swing positive, turning on the Darlington pair. Current flows from the +15V supply, through the battery pack and to ground via the 0.6Ω shunt. The voltage across the shunt rises to 1V, balancing the summing junction, and the amplifier servo controls about 1.6A through the battery pack. As the battery charges, it heats. This heat is picked up by the battery-mounted thermocouple. The temperature difference between the two thermocouples determines the voltage which appears at the amplifier's positive input. As battery temperature rises, this small negative voltage (1°C difference between the thermocouples equals 40μV) becomes larger. The amplifier, operating at a gain of 4300, gradually reduces the current through the battery to maintain its inputs at balance. The effect of this action is shown in Figure 4. The battery charges at a high rate until heating occurs and the circuit then tapers the charge. The values given in the circuit limit the battery surface temperature rise over ambient to about 5°C.

Precision Adjustable Dead Zone Circuit

Figure 5 details a precision adjustable dead zone circuit. This is particularly useful in motor driven position servo circuits. In such applications it is desirable to generate an adjustable, symmetrical dead band so that the servo motor's degree of stiffness and hunting characteristics around null may be controlled. In addition, because stages of this type are usually followed by very high gain servo amplifiers, it is necessary that low voltage offsets be maintained when inside the dead band zone.

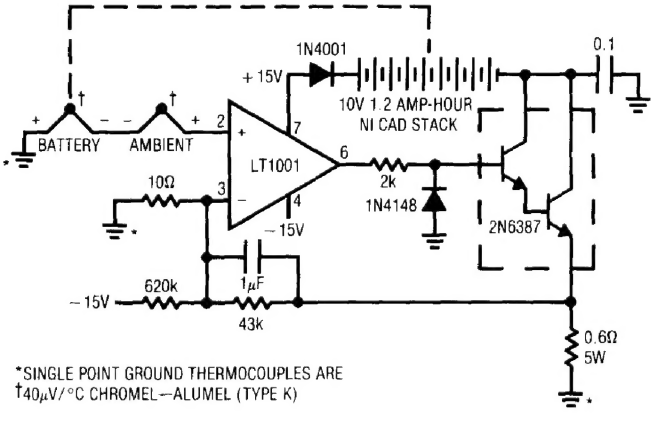


Figure 3. Thermally Controlled Ni Cad Battery Charger

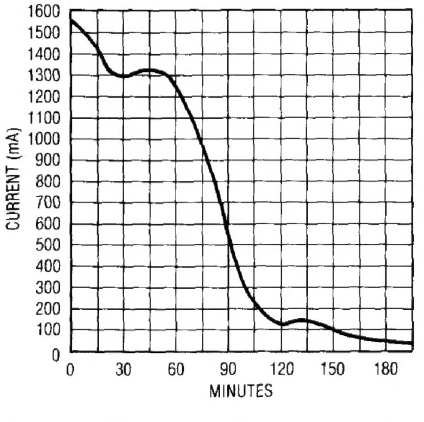


Figure 4. Charging Current vs Time for a 1.2A-Hour Cell

The circuit is made up of a synchronous rectifier (A1, C1), a variable unipolar dead zone cell composed of A2A and Q2–Q4, and a demodulator (A2B). When a circuit input (Trace A, Figure 6), in this case a triangle wave, is applied, the C1 crossing detector determines its polarity. C1's output (Trace B, Figure 6) drives Q1. When the input is negative, C1 goes high and Q1 conducts, grounding A1's positive input (Trace C, Figure 6). This turns A1 into a unity-gain inverter and its output (Trace D, Figure 6) inverts the input signal. For negative inputs, C1's output is low, cutting Q1 off and A1 unity-gain follows the input. This synchronous rectification presents the dead zone cell with a unipolar signal. Q2 forms a voltage adjustable current control at A2A's summing junction. Q3 provides V_{BE} temperature compensation and Q4 protects Q2's V_{BE} against reverse bias. When the dead zone command input is above A1's output, Q2 (Q2 emitter is Trace E, Figure 6) is off and A2A's output (Trace F, Figure 6) goes to zero. When A1's output rises above the dead zone input, Q2 conducts, A2A functions as a current-to-voltage converter, and an inverted version of A1's output appears at A2A's output. This signal feeds synchronous demodulator A2B, which recovers the bipolar input signal. Q6 is switched by Q5's phase inverted version of C1's output. When the circuit signal input is positive, Q6 is on, grounding A2B's positive input (Trace G, Figure 6) and A2B's output inverts. The opposite action occurs for negative signal inputs. In this fashion, A2B's output recovers the bipolar input signal while preserving the adjustable dead zone. Because the same device (Q2) is used for positive and negative signals, dead zone symmetry is nearly ideal. Q2's V_{BE} drop limits the minimum dead zone to 600mV. Thus, A1's offsets will never be seen when the circuit is in dead band and the effects of delay time and offset in C1 are similarly eliminated. Only A2A and A2B need to be low offset devices.

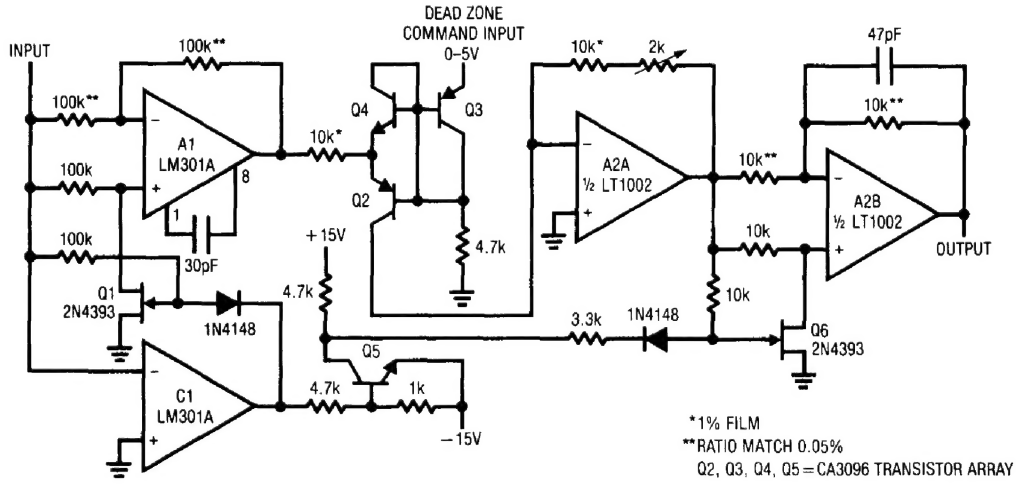


Figure 5. Precision Adjustable Dead Zone Generator

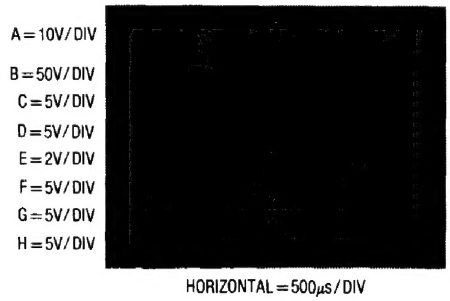


Figure 6

Ultra-Precision Variable Voltage Reference

Figure 7 combines an LT1002 with a MOSFET switched toroid to create a precision variable voltage reference with a wide dynamic range of outputs. The reference has two outputs. The low voltage range spans 0V to 10V and is settable in 100μV (10ppm at full scale) increments. The high voltage range runs from 0V to 100V in 1mV steps (also 10ppm at full scale). The low voltage range is derived from A1, the LM199A voltage reference, and the panel mounted Kelvin-Varley Divider (KVD). A1 is a follower with gain, with the 2N2219 used for a boosted output. The selected value, typically in the 43kΩ range, and the 100Ω potentiometer are used to trim the output to 10.0000V with the KVD dials set to full scale. The low offset of the LT1002 op amp eliminates the need for an offset trim. The non-inverting configuration used permits the 100kΩ KVD to be unloaded by the amplifier. The low bias current and high CMRR of the LT1002 are required to read the KVD without introducing error. The 100Ω resistor is a short circuit limit and the low range output is taken at the 2N2219 emitter.

The circuit achieves its high voltage output without resorting to separate high voltage power supplies. Instead, the DC input to a chopped step-up toroidal transformer is servo-controlled by an op amp. The C1 multivibrator generates a 40kHz clock, which is divided into a complementary 20kHz square wave by the 74C74 flip-flop. These waveforms bias the VMOS FETs. A2 compares the divided down output of the transformer's rectifier-filter against the low voltage output. The amplified difference voltage biases the power Darlington, which drives the transformer's primary center tap, completing a feedback loop around the transformer. The 0.1μF unit is used for loop stability. A2 servos whatever voltage is required to balance its inputs. The loop is calibrated so a precise 0V–100.00V output corresponds to the setting of the KVD dials. The VMOS choppers are the key to maintaining the wide dynamic range of settings on the high voltage scale. Their resistive saturation characteristic allows the control range to extend to within an LSB (1mV) of 0V. The 2N2907 serves as a simple coarse voltage clamp on the high voltage range. The potentiometer allows a voltage ceiling to

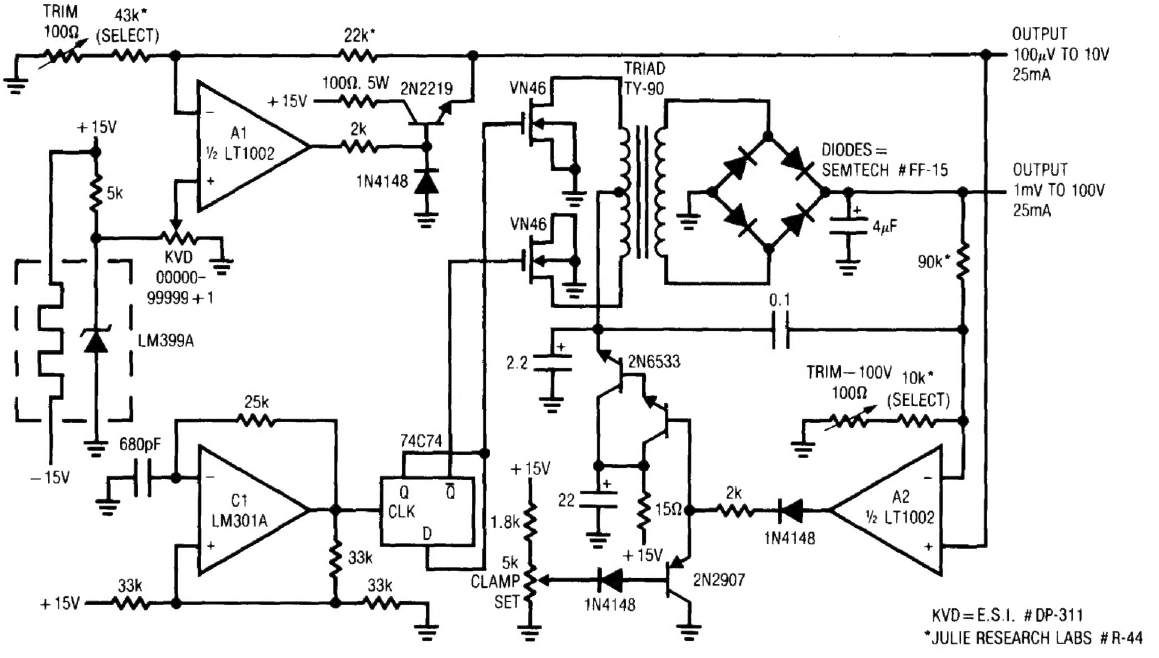


Figure 7. Ultra-Precision Variable Voltage Reference

be set for safety or other reasons when using the reference. To calibrate this circuit, select the 43kΩ value and adjust the 100Ω trim for a precise 10.0000V output at the low voltage output. Next, select the 10kΩ value and trim the 100Ω unit in the high voltage divider string. The typical stability of this circuit under laboratory conditions (25°C ± 5°C) may be estimated from the following data:

10V Range

Zener drift— temperature 5°C × 0.2ppm/°C	= 1ppm
Zener drift—time (per year)	= 25ppm
A1 op amp E_{OS} drift 0.5μV/°C × 5°C × A = 1.4 = 2.5μV	= 0.25ppm
A1 op amp E_{OS} drift— 1 year = 10μV/year	= 1ppm
KVD—2ppm/°C ratio shift × 5°C	= 10ppm
	37.25ppm over ± 5°C and 1 year at full scale

100V Range

All above errors	= 37.25ppm
A2 time and temperature	= 0.5ppm
	37.75ppm at full scale

Precision High Speed Op Amp

The design requirements to achieve high DC accuracy in an amplifier such as the LT1001/1002 preclude high speed performance. Additionally, it is difficult to design a precision monolithic amplifier which will drive large currents because of internal die heating problems. Some applications do call for speed, accuracy and output drive capability. Figure 8 shows a circuit which can be used to meet these conflicting requirements. In this arrangement, the LT1001 is used to stabilize a broadband stage to build an op amp with the DC precision of the LT1001 and high speed capability. This composite amplifier

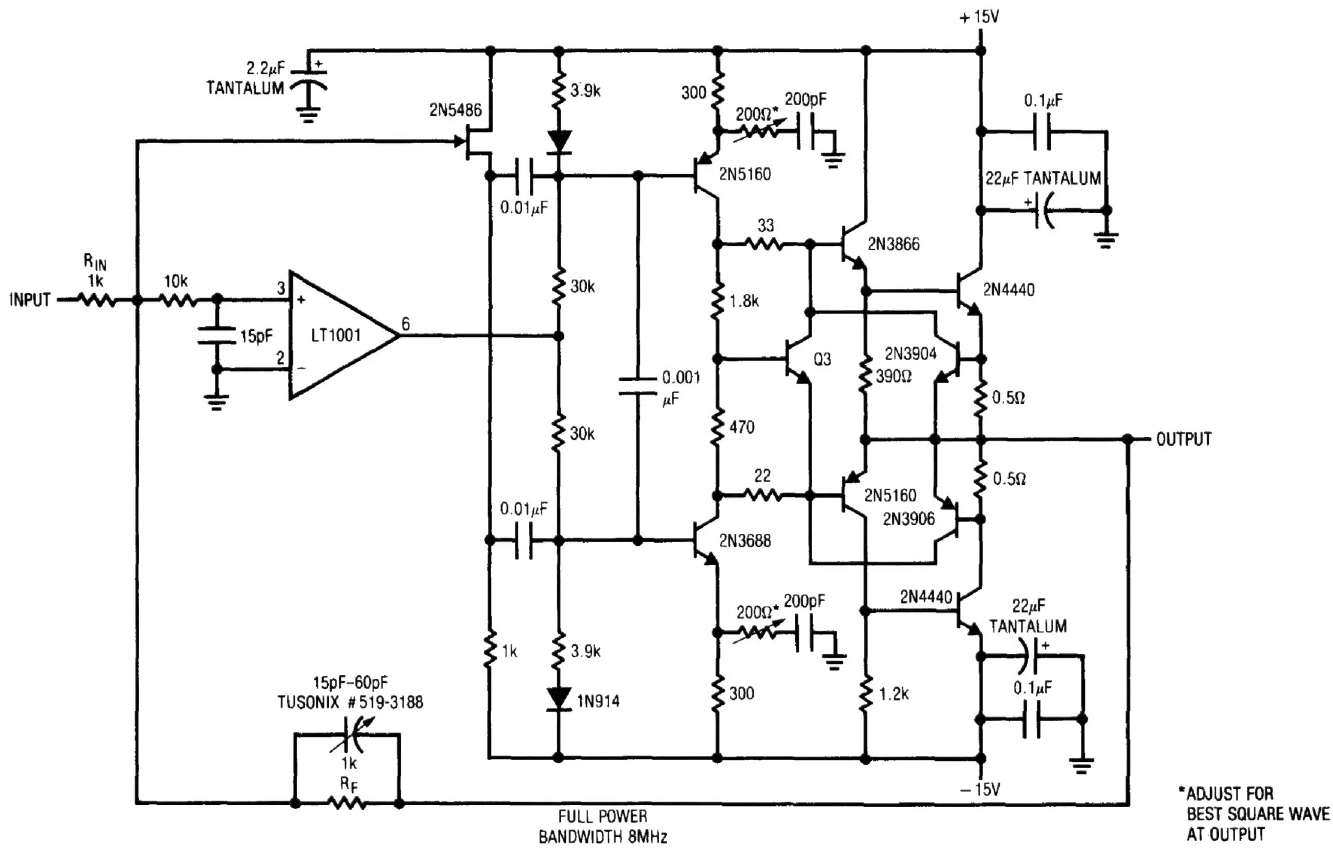


Figure 8. 1000V/μs 1A Op Amp

features a 1500V/μs slew rate, full output to 8MHz and will drive $\pm$10V into a 10Ω load. It is short circuit protected at $\pm$1A. The offset and drift specifications are controlled by the LT1001. High speed signals are fedforward around the LT1001 through Q10 and directly drive the wideband stage. The LT1001 operates at low frequency to DC stabilize the fast stage. The high frequency rolloff of the LT1001 is matched to the low frequency rolloff of the discrete stage.

The high speed stage is composed of transistors with Ft's approaching 1GHz. The output devices are NPN RF power transistors in a quasi-complementary arrangement. This is necessary because PNP RF power transistors are not available. Q8 and Q9 limit short circuit current by sensing across 0.5Ω shunts. They apply degenerative feedback around the output stage when turned on, thereby limiting current. The 200Ω potentiometers and the variable feedback capacitor should be adjusted for a compromise between slew rate and output waveform clarity. Typically, the highest slew rate will sacrifice clean transitions. Figure 9 shows the response of the amplifier (Trace B) to a fast input pulse (Trace A), with the adjustments optimized for clean transitions. Slew rate is still 1000V/μs and the output appears clean within the 275MHz bandpass of the monitoring oscilloscope. In setting up and using this circuit, RF layout techniques and a ground plane are mandatory and the 2N4440s must be heat sunk.

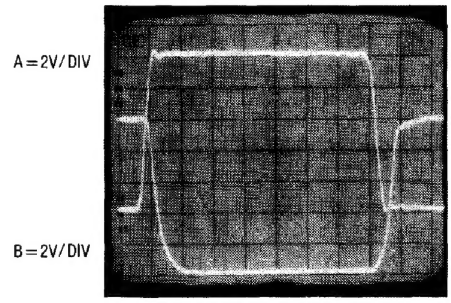


Figure 9. Op Amp Response